e-mentor

DWUMIESIĘCZNIK SZKOŁY GŁÓWNEJ HANDLOWEJ W WARSZAWIE WSPÓŁWYDAWCA: FUNDACJA PROMOCJI I AKREDYTACJ KIERUNKÓW EKONOMICZNYCH

2020, nr 2 (84)



Gapinski, A. J. (2020). A digital electronics course based on a hybrid delivery method using Digilent BASYS FPGA boards. *e-mentor*, *2*(84), 22–31. https://doi.org/10.15219/em84.1465



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A digital electronics course based on a hybrid delivery method using Digilent BASYS FPGA boards

Abstract

The article discusses the teaching methodology for a digital electronics course utilizing BASYS Field Programmable Gate Array (FPGA) boards (Digilent, Inc.), with a hybrid or blended classroom delivery method. The article outlines a methodology that combines the teaching of current digital circuit design technology with the use of a pedagogical approach to online delivery for a proportion of the course lectures. The FPGA boards by Digilent offer a modern PLD technology platform where beginners and more advanced practitioners alike may design and implement digital circuits with various operational capabilities. This means that the boards offer state-of-the art technology for computer engineering instructors to effectively introduce modern programmable memory technologies in the classroom. However, in light of the increased necessity for flexibility in college course delivery methods, the article also shows a successful method of material delivery that incorporates an online component. This aspect addresses the current expectations for greater course delivery flexibility and convenience due to the increasing number of adult students who need to work to support themselves and/or their families. Thus, the article offers an effective pedagogical approach to teaching current digital circuit analysis and design using a modern material delivery method.

Keywords: digital circuit design, hybrid or blended delivery method, programmable memory devices, computer engineering course, VHDL

Introduction

The last few decades have brought dramatic advances in engineering, especially in the area of digital technologies. Within this field, programmable logic devices (PLD) have played an increasingly important role in the design and implementation of digital circuits. While PLD platforms encompass a variety of different technologies, the field programmable gate array (FPGA) stands out currently as being the most advanced. The accompanying programming languages used to program PLDs and FPGAs underwent parallel advancements. These programming languages, known as hardware description languages (HDLs) (Hardware description language, n.d.), were adopted and have seen increasing acceptance through the years by engineering and industrial designers and practitioners alike. Regarding HDL platforms, it seems that VHDL has become the most dominant programming language used for programmable digital design and synthesis. There are already many resources on VHDL available in the literature, such as Sudhakar Yalamanchili (2005) or Peter Ashenden (2008).

Over the last three decades many researchers and academicians have written text-books on digital analysis and design, including Randy Katz and Gaetano Borriello (2004), Frank Scarpino (1998), David Van den Bout (1998), and Sunggu Lee (1999). However, only the more recent publications and textbooks (Widmer et al., 2017; Mano & Ciletti, 2018; or Haskell & Hanna, 2009) provide more complete exposure to analysis and design with PLD using a specific HDL programming language and selected PLD technology. A recent publication (Gapinski, 2018) discusses the digital design of the selected combinatorial and sequential circuits with the FPGA technology used by Digilent FPGA boards.

In considering the fast pace of change in the technology of digital circuits, it would seem that the pedagogy of teaching and learning have been left behind with the adoption of new material delivery methods. The university teaching processes,

confined to on-campus face-to-face sessions used since the beginning of the existence of higher learning institutions, have only relatively recently begun to adapt to market forces and the changing landscape of student expectations through the adoption of online teaching methods. One of these pedagogical methods of material delivery is a hybrid or blended form, which is understood here as "an educational approach that combines online instruction with face-to-face instruction," after Randy Garrison and Heather Kanuka (2004), and Mark Lamport and Randy Hill (2012). In the last decade or so the blended format approach has gained increasing adoption in universities and colleges in the USA, although the predominant method still remains the face-to-face form. See Betty Collis et al. (2003), Charles Dziuban et al. (2004), Garrison and Kanuka (2004), Lamport and Hill (2012), and Barbara Means et al. (2010). The worldwide events associated with the coronavirus pandemic changed the situation drastically and forced academic institutions to switch to online delivery completely in the spring of 2020, resulting in a more prevalent adoption of technological tools (Marcus, 2020). Naturally, those instructors who were already familiar with hybrid or blended methods in teaching were much better equipped to deal with the new circumstances, and switched to online delivery relatively more quickly.

Aliye Karabulut Ilgu and Charles Jahren (2015) analyzed the survey results of instructors who had extensive experience with hybrid teaching, concluding that hybrid learning provides such benefits as: flexibility, convenience, self-paced learning, improvement in student engagement and empowerment, free time for complex problem solving, and improved efficiency of classroom use at the institutional level. They list some of the difficulties experienced by the faculty they surveyed, including the time investment required for initial course development, reduced interaction with students, insufficient instructional/ institutional support, and technical issues associated with online delivery that had to be resolved. Interestingly, a meta-analysis of the effectiveness of online education by the U.S. Department of Education (Means et al., 2010) reported that students in an online learning environment performed modestly better than in a face-to-face environment, and that hybrid learning provided better results than both face-to-face and pure online methods. The metaanalysis by Means et al. (2010) was performed based on empirical studies in higher education of many disciplines such as: medical education, career technology, corporate and military training, and a small number of K-12 studies to ensure that the study was very broad in scope. As far as devising effective methodologies for online educational sessions, the study indicates that: "attempts to guide the online interactions of groups of learners were less successful than the use of mechanisms to prompt reflection and self-assessment on the part of individual learners." Thus, the study by Means et al. (2010, p. 48) suggests

that instructors, while preparing the pedagogical methodologies for online learning, should focus more on incorporating techniques that induce individual reflection and self-assessment by the learner than group interactions in order to achieve success in meeting the educational objectives. The main objective of the Means et al. (2010, p. xi) study was to "provide policy-makers, administrators and educators with research-based guidance on how to implement online learning for K-12 education and teacher preparation." In contrast, the author's experience was based exclusively on teaching and learning processes performed with engineering students. As far as the learning outcomes were concerned, the author did not observe any significant differences between the standard face-to-face and hybrid instruction methods. Thus, the author's experiences in teaching the course discussed here do not replicate the conclusions of Means et al. (2010). Furthermore, in the author's observations, e-learning is more suitable for more self-disciplined and motivated individuals with a better academic standing. The academically weaker students, based on the author's observations, need much more, if not entirely, face-to-face instruction to learn the material satisfactorily.

Consequently, the article discusses the teaching of digital circuit analysis and design using a hybrid delivery format. The course is a required freshman EET/EMET class that uses current FPGA technology with boards by Digilent, Inc. (www.digilentinc.com) in the digital design of selected combinatorial and sequential circuits with the VHDL programming language. By demonstrating how to introduce the most modern technology in the engineering/engineering technology curriculum using a blended method of delivery, the article provides the engineering faculty with an effective pedagogical methodology of introducing current programmable memory technology within a university program.

Hybrid or blended format as a course delivery method

Digital circuit design courses play an important role in electrical and computer engineering curricula at colleges and universities across the USA. Consequently, the instructors of digital design courses often face the issue of selecting a suitable material delivery methodology on top of selecting a current technology to be used for illustration and implementation of the designs. The digital design course material is usually delivered via lecture and accompanied by laboratory sessions. However, the recent decade or so has brought a new consideration in the selection of viable course delivery methods, namely the changing demographics of the student body. The latter features an increasing number of adult students who either work part-time or full-time, which brings to the fore the issue of how to accommodate them in the course content delivery process. The increasing number of adult working students within the

student body forces educational institutions and their instructors to seek new ways of accommodating student needs and to offer novel methods of material delivery with an online component (Collis et al., 2003; Dziuban et al., 2004; Gapinski, 2012; Garrison & Kanuka, 2004; Lamport & Hill, 2012; Means et al., 2010; Turula, 2017).

Recently, based on long experience with hybrid delivery in other engineering technology courses (see Gapinski, 2012, 2013), the author offered a digital circuit design class using a blended or hybrid format. Prior to the hybrid format, the standard face-to-face course delivery method meant meeting twice a week for a lecture and once a week for a laboratory session. With the new blended delivery method the first of the two weekly lecture sessions was delivered online via a synchronous mode. The online synchronous session was offered at the same time of day as the one taught on campus. The online sessions were recorded and available to students for retrieval online via a university course management system (Canvas). The second weekly lecture session and the accompanying laboratory session were held on-campus in face-to-face settings. As far as topical delivery breakdown was concerned, while the online sessions usually introduced the main concepts to the students, the face-to-face campus sessions were devoted to a more detailed analysis and practice. Consequently, as far as the material breakdown was concerned, about 40% of the lecture material was delivered online with the rest as on-campus delivery. For the online component, the author successfully used the Penn State University video-conferencing tool offered by Adobe Inc., and more recently the videoconferencing tool provided by Zoom. The video-conferencing tools allowed content delivery via a computer monitor, including an interactive drawing capability (used by both instructor and students) and chat/text boxes for the exchange of written information, which allowed the instructor to answer questions posted by the participating students, and vice versa. The author also used the interactive mode online occasionally to allow students to draw their concepts on the partitioned screen during the lecture or discussion sessions. The author, while preparing material for delivery, selected specific techniques that induced prompt reflection and self-assessment on the part of the individual learner (specific and open-ended questions, opening/closing reflective prompts, 3-2-1 technique (DASA, 2018)) during the online sessions.

Naturally, the interactive online mode was only manageable with a limited number of students (not exceeding 12–15). The author also used the videoconferencing tools to deliver ad-hoc help sessions to individual students at mutually agreeable time slots. The anonymous surveys showed positive appreciation of the hybrid delivery method, especially by commuting students who often indicated significant time savings by not having to travel to campus. The students in their written comments expressed an appreciation of

the flexibility and convenience offered by the hybrid method. As far as learning effectiveness and meeting the teaching objectives were concerned, the author did not notice any significant differences in either the comprehension of the material by students or the achievement of educational outcomes in comparison to traditional face-to-face teaching/learning scenarios. Consequently, the author's experience does not confirm the results of Means et al. (2010) described earlier. In general, the author's experience verifies the anecdotal evidence that e-learning, either as a component of class delivery or a wholly online mode, is better suited to students who are already self-disciplined, motivated and having a better academic standing.

FPGA boards by Digilent, Inc.

The FPGAs boards by Digilent, Inc. were used to implement the designs of combinatorial and sequential circuits. The boards hosted XILINX FPGA chips (www.xilinx.com). The specific boards were the BASYS 2 and 3, hosting Xilinx Spartan-3E FPGA and Xilinx Artix-7 FPGA, respectively. To design and program the chips on the BASYS 2 and 3 boards, the author used Xilinx ISE and Xilinx Vivado software platforms, respectively.

These modern boards hosted powerful FPGA chips by Xilinx, each of which provided hundreds of thousands of gates for high performance logic functions.

The BASYS 3 board offered improved hardware capabilities over the BASYS 2 board, with 15 times the number of logic cells (from 2,160 to 33,280) and 26 times more RAM (Random Access Memory) etc. The BASYS 3 had the following specifications (www. digilent.com):

- 33,280 logic cells in 5,200 slices (each slice contains 4 x 6-input LUTs (Look-up Tables) and 8 flip-flops);
- 1,800 Kbits of fast-block RAM;
- five clock management tiles, each with a phase-locked loop (PLL);
- 90 DSP slices;
- internal clock speeds exceeding 450 MHz;
- on-chip analog-to-digital converter (XADC);
- 16-user switches;
- 16-user LEDs;
- 5-user pushbuttons;
- 4-digit 7-segment display;
- 4 Pmod connectors: 3 standard 12-pin Pmod & 1 dual-purpose XADC signal / standard Pmod;
- 12-bit VGA output:
- USB-UART bridge;
- serial flash;
- Digilent USB-JTAG port for FPGA programming and communication;
- USB HID host for mice, keyboards, and memory sticks.

Pedagogy of teaching digital design

The digital circuit analysis and design curriculum in engineering and engineering technology education traditionally involved discrete integrated chips in the implementation process. As technology progressed, the PLD technology was adopted for implementing digital designs throughout academic engineering programs. However, the digital circuit design pedagogy remains an open field, where individual instructors have to choose the teaching methodologies to meet the student learning outcomes within the program and to take into account the students' programming background and skills. In addition, the instructors have to choose the pedagogy to match the available local campus hardware. Thus, an instructor has to devise effective pedagogical methodologies, which usually involves migrating from discrete integrated chips to PLD devices. Consequently, introductory digital design courses are usually more challenging for instructors, since the students in these courses have rarely been exposed to any type of prior programming experience.

Furthermore, instructors increasingly have to offer more flexibility in content delivery due to the changing demographics of the students. Consequently, depending on local circumstances, finding the most effective method of material delivery often involves, besides the face-to-face on-campus sessions, the inclusion of some type of e-learning component.

In his introductory digital design course, the author usually began the design implementations with discrete elements, and then migrated towards PLD devices throughout the semester work. The accompanying laboratory sessions, usually with teambased activities, allowed the students to learn from each other and to fill the gaps in their knowledge accordingly. Naturally, the pace of the transition from discrete chip technology to HDL programming and PLD implementation had to be devised carefully. While VHDL essentials could be introduced in the lecture format, involving both online and campus settings, the practical examples were discussed and reinforced in the laboratory sessions. The more advanced digital circuit design courses did not usually present such a challenge, since the students were already skillful and knowledgeable in specific HDL programming.

Later, due to the need to accommodate working students, the author began to deliver the course in a hybrid format. While the online sessions were devoted to the introduction of major concepts, the campus face-to-face sessions were much more detail oriented, involving the analysis and design aspects of the various circuits.

The following sections show the application of state-of-the-art FPGA boards in combinational and sequential circuit design and implementation. While the general concepts of the designs were introduced in online sessions, the subsequent campus sessions allowed the students to actually develop their designs and implement them using XILINX ISE / VIVADO software and FPGA boards by Digilent.

Digital electronics – course contents

Digital Electronics was a required course for freshman students in the Electrical Engineering Technology (EET) associate degree program and the Electro-Mechanical Engineering Technology (EMET) bachelor program at Penn State University. The purpose of the course was to teach the principles of digital electronics. The course duration was of fifteen weeks, for 3 credits with an accompanied laboratory class of 1 credit in a typical spring semester.

The material covered a variety of topics, including number systems, Boolean algebra, basic logic gates, logic circuits, flip-flops, registers, arithmetic circuits, counters, interfacing with analog devices, and computer memory with PLDs, as listed below:

- unsigned number systems including decimal, binary, octal, hex and base conversion;
- codes BCD, Gray, ASCII and parity;
- basic digital logic gates (AND/OR) and truth tables;
- Boolean algebra postulate and theorems, equation reductions and circuit implementations:
- DeMorgan's theorems NAND and NOR gates, and implementation:
- sum of product circuits;
- HDL: VHDL;
- Karnaugh map and circuit simplification;
- multiplexers, demultiplexers, decoders and other MSI circuits;
- basic SR Flip-Flops NAND & NOR implementations and limitations;
- D Latch, Clocked and Edge Triggered D Flip-Flops;
- Edge Triggered JK Flip-Flop;
- Ripple Counter;
- DAC & ADC principles;
- sequential logic synchronous counters, shift registers and basic state machine concepts;
- memory systems RAM, ROM, PROM, EEPROM, etc.;
- programmable memory: PAL, PLA, PLD devices w/FPGAs.

The material was delivered, as explained earlier, during face-to-face on-campus sessions and online synchronously for the lecture component. The accompanying laboratory sessions took place on the campus. All class material, including MS Power Point slides, recorded online sessions and additional materials on specific topics based on recent technological development, were available for student retrieval 24/7 via the university course management software. Course material comprehension assessment included written examinations, problem solving in both face-toface and online sessions, laboratory work on campus, written laboratory reports, participation in online sessions, and online timed quizzes. As far as material content delivery breakdown was concerned, about 40% of the lecture material was delivered online.

Digital circuit design examples

This section discusses two examples of digital design, as implemented with the FPGA BASYS 2 and 3 boards. As discussed earlier the design general themes of these two digital circuits were introduced in the online sessions and the design details were subject to face-to-face discussions in classroom settings. The first example illustrates the implementation of a 4-Bit Counter and the second example a 3-Line - To - 8-Line Decoder implemented with the BASYS 2 board and more advanced BASYS 3 board, respectively. The design work was then presented at the IEMS'2019 conference (Gapinski, 2019). For further details of the analysis and design of digital circuits with FPGA technology based on Digilent boards, see the book by Haskell and Hanna (2009) and the more recent book by Andrzej Gapinski (2018). VHDL code was used for the design work.

Example 1 - a 4-bit counter

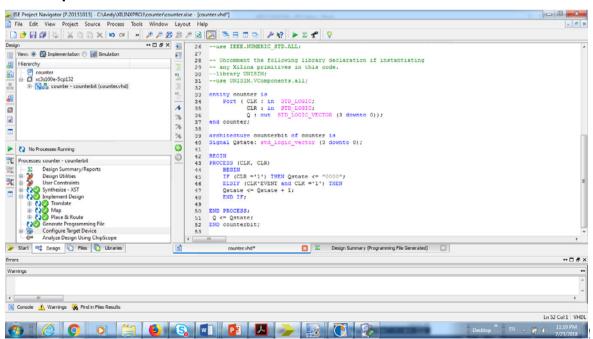
The following VHDL code was used for the counter synthesis (see Listing 1).

For the synthesis process, compilation, simulation, and chip programming, see Figures 1–5 below.

Listing 1. 4-bit counter VHDL code

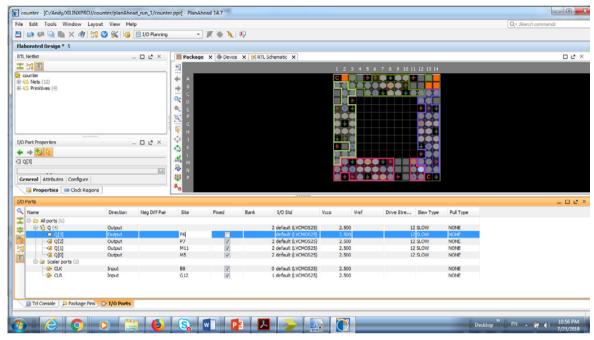
```
Library IEEE;
Use IEEE.std_logic_1164.all;
Use IEEE.std_logic_unsigned.all;
ENTITY counter IS
Port (CLK: in STD_LOGIC;
     CLR: in STD_LOGIC;
     Q: out STD_LOGIC_VECTOR (3 downto 0);
END counter;
ARCHITECTURE counterbit OF counter IS
SIGNAL Qstate: STD_LOGIC_VECTOR (3 downto 0);
BEGIN
PROCESS (CLK, CLR)
  BEGIN
      IF (CLR = '1') THEN Ostate <= "0000";</pre>
  ELSIF (CLK'EVENT and CLK ='1') THEN
      Qstate <= Qstate +1;
  END if:
END PROCESS;
Q <= Qstate;
END counterbit;
```

Figure 1. Xilinx ISE Project Navigator screenshot with VHDL code of the counter and successful synthesis performed as indicated in the process window



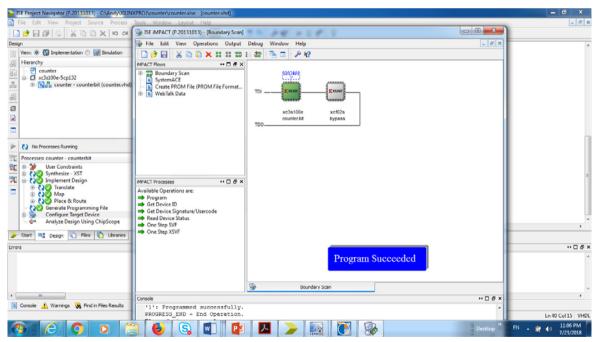
Source: Xilinx ISE Project Navigator.

Figure 2. ISE PlanAhead. UCF file. Pin assignments



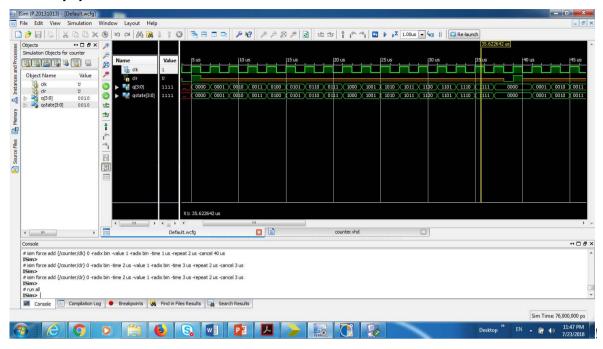
Source: ISE Software.

Figure 3. ISE synthesis successful. iMPACT used for downloading bit file



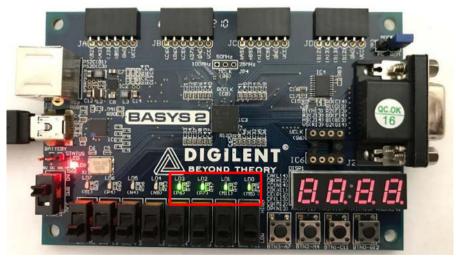
Source: ISE Software.

Figure 4. ISE ISim Simulator screenshot showing simulation of the 4-bit counter. Clock period set at T = 2us. A successful count is displayed



Source: ISE ISim Simulator.

Figure 5. BASYS 2 board. 4-bit counter. Screenshot shows illumination of four LEDs as outputs



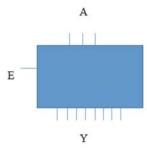
Source: Digilent Inc.

Example 2 - a 3-line to 8-line decoder

In this exercise a generic 3 x 8 decoder depicted in Figure 6 was implemented.

A 3 x 8 decoder has 3 x input lines (A = A2 A1 A0), enables line E, and 8 x output lines (Y = Y7Y6Y5Y4Y3Y2Y1Y0). When enabled, a decoder activates one output line depending on the binary value of the inputs. For example, if input line A = 010, the decoder activates output Y2 while keeping all remaining outputs disabled. For the VHDL code for this decoder, see Listing 2.

Figure 6. Model of 1-of-8 decoder



A digital electronics course based on a hybrid delivery...

Listing 2. Decoder VHDL code

```
ENTITY Decoder IS
  PORT (A: in STD_LOGIC_VECTOR (2 downto 0);
      EN: in STD_LOGIC;
      Y: out STD_LOGIC_VECTOR (7 downto 0));
END Decoder:
ARCHITECTURE Behavioral OF Decoder IS
SIGNAL inputs: STD_LOGIC_VECTOR (3 DOWNTO 0);
BEGIN
inputs <= EN & A;
  WITH inputs SELECT
     Y <= B"00000001" WHEN B"1000", -- Y0 active
        B"00000010" WHEN B"1001", -- Y1 active
        B"00000100" WHEN B"1010", -- Y2 active
        B"00001000" WHEN B"1011", -- Y3 active
        B"00010000" WHEN B"1100", -- Y4 active
        B"00100000" WHEN B"1101", -- Y5 active
        B"01000000" WHEN B"1110", -- Y6 active
        B"10000000" WHEN B"1111", -- Y7 active
        B"00000000" WHEN OTHERS; -- Decoder disabled
END Behavioral;
```

The decoder implementation is shown in the following figures with the simulation screenshot shown in Figure 7 and the implementation using board in Figure 8, respectively.

Table 1 shows the LEDs (outputs) (labeled L15,...,L0), the toggle switches (inputs) (labeled S15,...,S0) and their logic states (L7,..., L0 and S15, S2, S1, S0 used in the example) representing the LEDs and switches shown on the BASYS 3 board in Figure 8, inside the marked box.

The 3 x 8 decoder has three input lines, A = A2A1A0(switches S2, S1, S0), and enable line En (switch S15). Hence only the S15, S2, S1, S0 toggle switches are used for inputs. The decoder's eight output lines (Y7,..., Y0) are connected to board's eight LEDs (L7,..., L0), respectively. In the decoder example for input lines A2A1A0 = 011, with enable signal En = 1, the decoder activates output line Y3 connected to LED L3, as expected.

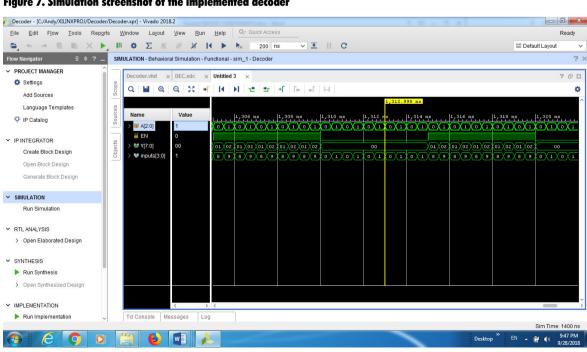


Figure 7. Simulation screenshot of the implemented decoder

Source: XILINX Software.

Figure 8. BASYS 3 board (with permission from Digilent, Inc.). Marked box shows the toggle switches as inputs (bottom row) and the LEDs above the last row as the outputs



Source: Digilent, Inc.

Table 1. Diagram of the BASYS 3 board LEDs (L16,..., L0) and toggle switches (S15,..., S0) — bottom part of the board, inside the marked box shown in Fig. 8

LED State									Off	Off	Off	Off	On	Off	Off	Off
LED	L15	L	L	L	L	L	L	L	L7	L6	L5	L4	L3	L2	L1	LO
State	On													Off	On	On
Switch	S15	S	S	S	S	S	S	S	S	S	S	S	S	S2	S1	S0
Role	En													A2	A1	A0

Source: author's own work.

Conclusion

The objective of the article was two-fold: to present teaching examples of digital circuit analysis and design with the application of Digilent boards hosting Xilinx FPGA programmable chips and to discuss the hybrid or blended teaching delivery method used by the author. The current technology of programmable memories is being applied in engineering curriculum nationwide and consequently provides a pedagogical challenge to instructors concerning the most effective methods for subject coverage and delivery method, whether face-to-face or in a hybrid format with some element of e-learning.

The author in freshman-level digital design courses began with traditional discrete chip technologies and migrated towards PLDs with FPGAs through the semester work. Naturally, the pace of transition was usually dictated by the level of the course, either introductory or more advanced, and also by the prior exposure of the students to programming languages, including VHDL. The online component was usually used to deliver about 40% of the material focused on the introduction of general concepts, with face-to-face on-campus sessions to deliver the rest of the material in a more detail-oriented analysis.

As far as achieving teaching/learning objectives and the students' comprehension of the material were concerned, the author did not notice any significant difference between the standard complete face-to-face on-campus course delivery conducted in earlier years and the blended or hybrid format. In that, the author's experience did not confirm the results of the meta-analysis of the effectiveness of online education reported by Means et al. (2010). In the anonymous class survey, the students in their comments expressed appreciation of the flexibility and convenience offered by the blended form of course delivery.

The article shows how material related to digital circuit analysis and design courses can be taught effectively using hybrid or blended forms of course delivery. As such, the article addresses the increasingly important factor faced by higher learning institutions of how to respond effectively to the changing demographics of current students and their expectations for more flexibility in the learning modalities offered by a university.

Acknowledgment

The author would like to thank Digilent, Inc. Corporation for providing permission to publish images and specification data.

A digital electronics course based on a hybrid delivery...

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Registration is open for the OASPA 2020 Conference which will take place online during the week of **Monday 21 – Friday 25 September 2020**. To register please go to the **registration page**. The full program will be announced soon. Further details will be available as soon as possible on the conference webpage, or you can sign up for updates if you would like the organizers to send you information updates as they become available. This year, the conference will start with a moderated discussion "Open access at a time of global challenge: How has the world changed." More information at **https://oaspa.org/conference/**